IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Charles F. Marino	**Conf. No.:**	4278
Serial No.:	10/057,817	**Art Unit:**	2628
Filing Date:	01/22/2002	**Examiner:**	CHOW, Jeffery J.
Title:	ENHANCED BLENDING UNIT PERFORMANCE IN GRAPHICS SYSTEM	**Docket No.:**	END920010104US1 (IBME-0036)

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Commissioner for Patents
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BRIEF OF APPELLANT

This is an appeal from the Final Rejection (Office Action) dated November 24, 2006, rejecting claims 1, 3-8, 10-13 and 15-18. The requisite fee set forth in 37 C.F.R. §1.17 (c) was submitted on February 26, 2007.

REAL PARTY IN INTEREST

International Business Machines Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There is no related appeal or interference.

STATUS OF CLAIMS

As filed, this case included claims 1-18. Claims 1, 3-8, 10-13 and 15-18 remain pending, stand rejected, and form the basis of this appeal. Claims 2, 9 and 14 have been cancelled. No claim has been allowed. The rejections of claims 1, 3-8, 10-13 and 15-18 are being appealed.

STATUS OF AMENDMENTS

No amendment has been proposed following the Final Rejection of November 24, 2006.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 provides a method of blending at least two images using a blending unit (36 of FIG. 2) in a graphics engine (22 of FIG. 1), the blending unit (36) including a plurality of multipliers (70 of FIG. 2), the method comprising: receiving a request for blending the at least two images (page 9, lines 1-2), each image having a pixel format (Id.); and reconfiguring each blending unit multiplier to perform at least two operations per multiplier per cycle (page 9, lines 3-4), wherein the reconfiguring includes bit slicing each multiplier according to the pixel format (page 9, lines 5-6).

Independent claim 8 provides a graphics system (30 of FIG. 1) having a blending unit (36), the blending unit (36) comprising: a plurality of multipliers (70 of FIG. 2); and a reconfiguration module (72 of FIG. 2) that reconfigures each multiplier of the blending unit to perform at least two operations per multiplier per cycle (page 9, lines 3-4), wherein the reconfiguration module (72) bit slices each multiplier according to a pixel format (page 8, lines 1-6; page 9, lines 5-6).

Independent claim 13 provides a digital video system (10 of FIG. 1) comprising: a

processor (14 of FIG. 1); a memory (12 of FIG. 1); an application (24 of FIG. 1) resident in memory (12); and a graphics system (30 of FIG. 1) for generating graphics, the graphics system including: a blending unit (36 of FIG. 2) including a plurality of multipliers (70 of FIG. 2), and means (72 of FIG. 2) for reconfiguring each multiplier of the blending unit to perform at least two operations per multiplier per cycle (page 9, lines 3-4), wherein the reconfiguring means bit slices each multiplier according to a pixel format (page 8, lines 1-6; page 9, lines 5-6).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1, 3 – 6, 8, 10 – 13 and 15 – 17 are anticipated under 35 U.S.C. §102(b) by U.S. Pat. No. 5,935,198, hereinafter "Blomgren".

2. Whether claim 7 is unpatentable under 35 U.S.C. 103(a) over Blomgren in view of US Pat. No. 5,912,832, hereinafter "Flahie", and US Pat. No.5,612,710, hereinafter "Christensen".

3. Whether claim 18 is unpatentable under 35 U.S.C. 103(a) over Blomgren in view of US Pat. No. 5,838,387, hereinafter "Allen".

ARGUMENTS

1. Claims 1, 3 – 6, 8, 10 – 13 and 15 – 17 are not anticipated by Blomgren

With respect to independent claims 1, 8 and 13, Appellant submits that Blomgren does not disclose, *inter alia*, "reconfiguring each blending unit multiplier … wherein the reconfiguring includes bit slicing each multiplier according to the pixel format." (Claim 1, similarly claimed in claims 8 and 13). Blomgren only discloses dividing a 32-bit multiplier (or a

64-bit multiplier) into 4 independent 8-bit sections (or four 16-bit sections for the 64-bit multiplier), but does not include reconfiguring the 32-bit multiplier (or a 64-bit multiplier) by bit slicing according to the pixel format of an image. Blomgren only expects images with color components of 8-bit size or 16-bit size. (Col. 13, lines 29-31). For images of the two color components sizes (i.e., 8-bit size or 16-bit size), Blomgren uses two sizes of multipliers to interpolate the color components, respectively. That is, Blomgren uses a 64-bit multiplier with four 16-bit sections to interpolate images with 16-bit color components and uses a 32-bit multiplier with four 8-bit sections to interpolate images with 8-bit color components. (Col. 13, lines 32-35 and 39-41). Blomgren does not disclose bit slicing a same multiplier according to different pixel formats. For example, Blomgren does not disclose bit slicing two 32-bit multipliers each into two 16-bit sections to interpolate a 64-bit image with 16-bit color components. Actually, in Blomgren, the "smaller sections" (col. 13, line 33) within a multiplier are "independent", and fixed, and can only be added "together as one large multiplier" (col. 13, lines 34-35). Blomgren does not disclose reconfiguring a multiplier according to the pixel format of an image.

In the Advisory Action of 2/14/07, the Examiner asserts that dividing a 32-bit multiplier into four smaller sections to interpolate four color components of 8-bit sizes discloses the above feature. (Advisory Action at page 2). Appellant respectfully disagrees. Blomgren does not disclose/expect an image with color components of 32-bit size (i.e., 128 total bits for 4 components), as such the whole 32-bit section of a 32-bit multiplier is only used for general purposes - not for graphics interpolations. (*See*, e.g., col. 13, lines 28-32.) Blomgren will divide a 32-bit multiplier (or a 64-bit multiplier) into four 8-bit sections (or four 16-bit sections in the case of the 64-bit multiplier) for graphics interpolations no matter what pixel format the image is.

That is, the division of the 32-bit multiplier will not change due to different image pixel formats. As such, Blomgren does not reconfigure each blending unit multiplier according to the pixel format of the image. Note that the change from 32-bit to four 8-bit sections is not a reconfiguration according to different pixel formats because the whole 32-bit section of the 32-bit multiplier is not used for interpolating components of an image. In view of the foregoing, Blomgren does not anticipate the claimed invention, and Appellant respectfully requests reversal of the final rejection.

In addition, Blomgren does not disclose, *inter alia*, "blending the at least two images[.]" (Claim 1, similarly claimed in claims 8 and 13). Instead, Blomgren only discloses interpolating the color components of a single image. (*See*, e.g., Abstract; see also col. 13, lines 36-38.) As such, Blomgren does not anticipate the claimed invention, and Appellant respectfully requests reversal of the final rejection.

The dependent claims are believed allowable for the same reasons, as well as for their own additional features.

2. Claim 7 is not obvious over Blomgren in view of Flahie and Christensen

The above arguments regarding claim 1 also apply to claim 7, and Flahie and Christensen do not overcome the above identified deficiencies of Blomgren.

3. Claim 18 is not obvious over Blomgren in view of Allen

The above arguments regarding claim 13 also apply to claim 18, and Allen does not overcome the above identified deficiencies of Blomgren.

In view of the foregoing, Appellant submits that the final rejection is defective, and should be reversed.

Respectfully submitted,

/Spencer K. Warnick/

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CLAIMS APPENDIX

1. A method of blending at least two images using a blending unit in a graphics engine, the blending unit including a plurality of multipliers, the method comprising:

receiving a request for blending the at least two images, each image having a pixel format; and

reconfiguring each blending unit multiplier to perform at least two operations per multiplier per cycle, wherein the reconfiguring includes bit slicing each multiplier according to the pixel format.

3. The method of claim 1, wherein the step of bit slicing includes bit slicing each multiplier to accommodate a first bits/pixel parameter of the pixel format.

4. The method of claim 3, wherein the step of bit slicing includes bit slicing each multiplier to accommodate a second bits/pixel parameter of the pixel format.

5. The method of claim 3, wherein the first bits/pixel parameter is a highest bits/pixel parameter of the pixel format.

6. The method of claim 5, wherein the highest bits/pixel parameter is no higher than 8 bits/pixel and no less than 1 bit/pixel.

7. The method of claim 1, wherein each blending unit multiplier is an 8-

bit by 8-bit multiplier.

8. A graphics system having a blending unit, the blending unit comprising:

a plurality of multipliers; and

a reconfiguration module that reconfigures each multiplier of the blending unit to perform at least two operations per multiplier per cycle, wherein the reconfiguration module bit slices each multiplier according to a pixel format.

10. The graphics system of claim 8, wherein the reconfiguration module bit slices each multiplier to accommodate a first bits/pixel parameter of a pixel format, and then a second bits/pixel parameter of the pixel format.

11. The graphics system of claim 8, wherein the blending unit is part of a graphics engine.

12. The graphics system of claim 8, wherein the graphics engine further comprises at least one of a raster operator, a color key operator, a pixel bit mask operator, a patter write mask operator and a pixel boundary modify write operator.

13. A digital video system comprising:

a processor;

a memory;

an application resident in memory; and

a graphics system for generating graphics, the graphics system including:

a blending unit including a plurality of multipliers, and

means for reconfiguring each multiplier of the blending unit to perform at least two operations per multiplier per cycle, wherein the reconfiguring means bit slices each multiplier according to a pixel format.

15. The system of claim 13, wherein the means for reconfiguring bit slices each multiplier to accommodate a first bits/pixel parameter of the format, and then a second bits/pixel parameter of the format.

16. The system of claim 13, wherein the means for reconfiguring is part of a graphics engine.

17. The system of claim 16, wherein the graphics engine further comprises at least one of a raster operator, a color key operator, a pixel bit mask operator, a pattern write mask operator and a pixel boundary modify write operator.

18. The system of claim 13, wherein the graphics system further comprises a scaler.

EVIDENCE APPENDIX

There is no evidence submitted.

RELATED PROCEEDINGS APPENDIX

There is no related proceeding.

CERTIFICATE OF SERVICES

There is no other party to this appeal proceeding.